CLAIMS

1. A process that uses a first processor, the process comprising:

blocking by the first processor of completion by a second processor of a configuration cycle; and

selecting, by the first processor, of one procedure from a plurality of procedures that are associated with respective types of circuitry that, if available to the first processor, permit the first processor to control a device, the one procedure being associated with one of the respective types of circuitry that is actually available to be used by the first processor.

2. The process of claim 1, wherein the selecting of the one procedure comprises:

causing a request to be issued; and

analyzing a response to the request.

3. The process of claim 2, wherein:

the response comprises a data word issued in response to the request; and

the analyzing of the response comprises:

comparing the data word to predetermined data words that respectively correspond to the types of circuitry.

4. The process of claim 3, wherein:

the predetermined data words comprise respective identification numbers associated with the types of circuitry.

5. The process of claim 3, wherein:

the data word issued in response to the request identifies the device and a vendor of the device.

6. A circuit card comprising:

a connector to be coupled to a slot in a circuit board;

circuitry to be coupled via the connector to a bus in the circuit board when the connector is coupled to the circuit board;

the circuitry being operable, when the circuitry is coupled via the connector to the bus, to perform operations including:

preventing completion by a processor coupled to the bus of a configuration cycle involving a device that is also coupled to the bus, the processor and the device being external to the circuit card; and

selecting one procedure from a plurality of procedures that are associated with respective types of mechanisms that, if available to be used by the circuitry, permit the circuitry to control the device, the one procedure being associated with one of the respective types of mechanisms that is actually available to be used by the circuitry.

7. The circuit card of claim 6, wherein the circuitry is also operable, when the circuitry is coupled via the connector to the bus, to use the one procedure to perform a configuration operation to facilitate control of the device by the circuitry.

8. The circuit card of claim 6, wherein the device comprises an input/output (I/O) device comprised in the circuit board.

9. The circuit card of claim 8, wherein the I/O device comprises one of a data storage controller, a network data communication controller, and a server management controller.

10. The circuit card of claim 8, wherein the I/O device comprises a data storage controller to control one or more storage devices.

11. The circuit card of claim 10, wherein the data storage controller is able to communicate with the one or more storage devices using one of a Fibre Channel protocol, a Serial-ATA protocol, a Small Computer System Interface protocol, and an Ethernet protocol.

12. The circuit card of claim 10, wherein the one procedure, when implemented, permits the circuitry to configure the one or more storage devices as a redundant array of independent disks (RAID).

13. The circuit card of claim 6, wherein:

the circuit board is a motherboard;

the bus comprises one of a Peripheral Component Interconnect (PCI) bus and a PCI-extended (PCI-X) bus; and

the connector is insertable into the slot.

14. The circuit card of claim 6, wherein:

the processor comprises a host processor on the circuit board;

the circuitry comprises an input/output (I/O) processor and a memory; and

the memory is to store a set of program instructions that when executed by the I/O processor, cause the operations to be performed by the circuitry.

15. The circuit card of claim 6, wherein:

the types of mechanisms that may be used to permit the circuitry to control the device include modular redundant array of inexpensive disks (RAID) on motherboard (MROMB) control mechanisms.

16. Circuitry comprising:

a first processor to block completion by a second processor of a configuration cycle, to select one procedure from a plurality of procedures that are associated with respective types of mechanisms that, if available to be used by the first processor, permit the first processor to control a device, the one procedure being associated with one of the respective types of mechanisms that is actually available to be used by the first processor.

17. The circuitry of claim 16, wherein:

the first processor is configured to select the one procedure by causing a request to be issued and by analyzing a response generated in response to the request.

18. The circuitry of claim 17, wherein:

the response comprises a data word; and

the first processor is configured to compare the data word to a plurality of predetermined data words corresponding to the respective types of mechanisms.

19. The circuitry of claim 18, wherein:

the predetermined data words comprise respective identification numbers associated with the types of mechanisms.

20. The circuitry of claim 18, wherein:

the data word issued in response to the request identifies the device and a vendor of the device.

21. A process that uses a circuit card, the circuit card including a connector and circuitry coupled to the connector, the process comprising:

coupling the connector to a slot in a circuit board, the coupling of the connector to the slot causing the circuitry to become coupled via the connector to a bus in the circuit board; and

when the circuitry is coupled to the bus, the circuitry performs operations including:

preventing completion by a processor coupled to the bus of a configuration cycle involving a device that is also coupled to the bus, the processor and the device being external to the circuit card; and

selecting of one procedure from a plurality of procedures that are associated with respective types of mechanisms that, if available to be used by the circuitry, permit the circuitry to control the device, the one procedure being associated with one of the respective types of mechanisms that is actually available to be used by the circuitry.

22. The process of claim 21, wherein, when the circuitry is coupled to the bus, the circuitry also carries out the procedure.

23. The process of claim 21, wherein the device comprises a data input/output (I/O) device comprised in the circuit board.

24. The process of claim 23, wherein the I/O device comprises one of a data storage controller, a network data communication controller, and a server management controller.

25. The process of claim 23, wherein the I/O device comprises a data storage controller to control a set of one or more storage devices.

26. The process of claim 25, wherein the data storage controller communicates with the set of storage devices using one of a Fibre Channel protocol, a Serial-ATA protocol, a Small Computer System Interface protocol, and an Ethernet protocol.

27. The process of claim 25, wherein the procedure, when implemented, permits the circuitry to configure the set of storage devices as a redundant array of independent disks (RAID).

28. The process of claim 21, wherein:
the circuit board is a motherboard;
the bus comprises one of a Peripheral Component Interconnect (PCI) bus and a PCI-extended (PCI-X) bus; and
the connector may be inserted into the slot.

29. The process of claim 21, wherein:
the processor is a host processor comprised in the circuit board;
the circuitry comprises an input/output (I/O) processor and a memory; and
the process further comprises:

storing in the memory a set of program instructions that when executed by the I/O processor, cause the operations to be performed by the circuitry.

30. The process of claim 21, wherein:

the types of mechanisms include modular redundant array of inexpensive disks (RAID) on motherboard (MROMB) control mechanisms.

31. Memory that stores program instructions that when executed by a first processor cause the first processor to perform operations comprising:

blocking by the first processor of completion by a second processor of a configuration cycle; and

selecting of one procedure from a plurality of procedures that are associated with respective types of circuitry that, if available to be used by the first processor, permit the first processor to control a device, the one procedure being associated with one of the respective types of circuitry that is actually available to be used by the first processor.

32. The memory of claim 31, wherein the determining of the type of the device by the first processor comprises:

causing a request to be issued; and

analyzing a response to be generated to the request.

33. The memory of claim 32, wherein:

the response comprises a data word issued in response to the request; and

the analyzing of the response comprises:

comparing the data word to predetermined data words corresponding to the types of circuitry.

34. The memory of claim 33, wherein:

the predetermined data words comprise respective identification numbers associated with the types of circuitry.

35. The memory of claim 33, wherein:

the data word issued in response to the request identified the device and a vendor of the device.

36. The memory of claim 33, wherein the memory comprises at least one memory selected from the group consisting of: a semiconductor memory, a programmable memory, a non-volatile memory, a read only memory, an electrically programmable memory, and a disk memory.

37. A circuit board comprising:

a processor, a connector slot, a device, and a bus, the connector slot being to receive a circuit card, the circuit card including circuitry to be coupled via the connector slot to the bus when the circuit card is received by the connector slot;

the circuitry being operable, when the circuitry is coupled via the connector slot to the bus, to perform operations including:

preventing completion by the processor of a configuration cycle involving the device, the device being coupled to the bus; and

selecting of one procedure from a plurality of procedures that are associated with respective types of mechanisms that, if available to be used by the circuitry, permit the circuitry to control the device, the one procedure being associated with one of the types of mechanisms that is actually available to be used by the first processor.

38. The circuit board of claim 37, wherein:

the processor comprises a host processor;

the device comprises one of a data storage controller, a network data communication controller, and a server management controller;

the circuitry comprises an input/output (I/O) processor and a memory; and

the memory is to store a set of program instructions that when executed by the I/O processor, cause the operations to be performed by the circuitry.

39. A system comprising:

a circuit board comprising a bus and modular redundant array of inexpensive disks on motherboard (MROMB) hardware;

a device coupled to the data bus through the MROMB hardware; and

circuitry, coupled to the bus, to identify a type of the hardware and, based upon the type of the hardware, to control the hardware to implement a MROMB technique that may be implemented using the hardware.

40. The system of claim 39, wherein:

the circuit board comprises a host processor;

the device comprises one of a data storage controller, a network data communication controller, and a server management controller;

the circuitry comprises an input/output (I/O) processor and a memory; and

the memory is to store a set of program instructions that when executed by the I/O processor, cause the operations to be performed by the circuitry.